HT82012

ADPCM Synthesizer for External Serial ROM

Features

- Operating voltage: 2.4V~5.0V
- Direct interface with the HOLTEK serial ROM
- 12-bit ayalysis and 3-bit/4-bit ADPCM coding algorithm
- A maximum of 16 keys
- Auto power control for external power amplifier
- Programmable for FLAG:
  - End-pulse output
  - Busy output
- Programmable for voice sampling rate (4K~8K)
- KEY0 as a stop key
- External serial ROM size up to 1Mb×8/ 512Kb×8
- Programmable for KEYs:
  - Sequential (only for KEY1)
  - Retriggerable (for KEY1~KEY15)
  - Nontriggerable (for KEY1~KEY15)
  - Level Hold (for KEY1~KEY15)
  - Play one time and auto stop
  - Repeat and non-stop
- 3.58MHz crystal oscillator or resonator for system clock (VDD=5V)
- Voice capacity:
  456s—1Mb×8 ROM, 6K sampling rate, 3 bit format
  342s—1Mb×8 ROM, 6K sampling rate, 4 bit format

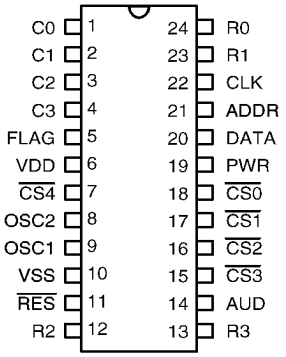
Applications

- Toys
- Alarm clocks
- Public address system
- Alert & warning system
- Sound effect generators
- Production with voice interface

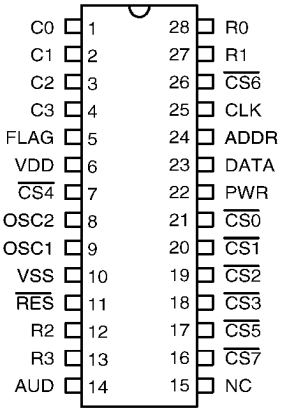
General Description

The HT82012 is a 3-bit/4-bit ADPCM voice synthesizer LSI implemented in CMOS technology. It provides an external serial ROM interface circuit and 16 matrix keys operation. The size of the voice ROM is decided by the type (512K or 1M) and number of the external ROM (up to 8 at maximum). The customer's voice sources are encoded into 3-bit/4-bit format and saved in the external voice ROM by the HOLTEK tools. The instructions of section play-back arrangemant for each key are stored in the table ROM. Also the key features are programmable. With such a flexible structure, the HT82012 is excellent for versatile voice applications.

Pin Assignment

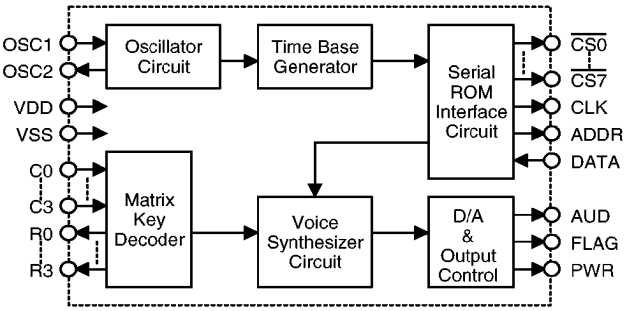


HT82012
– 24 SDIP/SOP

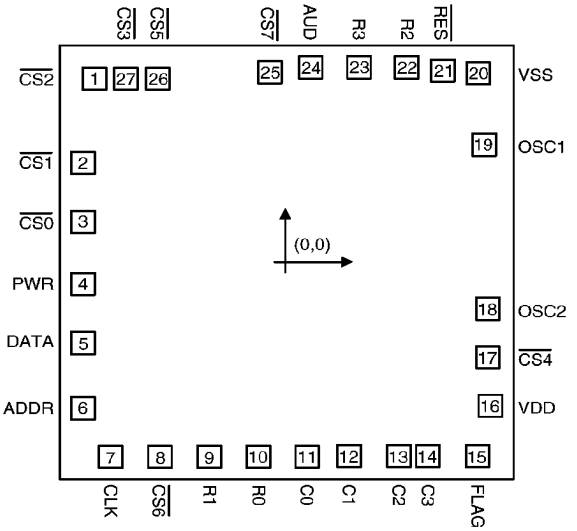


HT82012
– 28 SDIP/SOP

Block Diagram



Pad Coordinates



Chip size: 2980×2550 $(\mu m)^2$

* The IC substrate should be connected to VSS in the PCB layout artwork.

Unit: μm

Pad No.	X	Y	Pad No.	X	Y
1	–1224.25	988.5	15	1227.25	–1045.0
2	–1296.25	535.5	16	1312.25	–774.0
3	–1296.25	217.5	17	1295.75	–513.0
4	–1296.25	–119.0	18	1296.25	–252.0
5	–1296.25	–437.0	19	1273.25	635.0
6	–1296.25	–789.5	20	1234.75	1018.0
7	–1120.25	–1050.0	21	1007.75	1034.5
8	–804.75	–1050.0	22	777.75	1050.0
9	–490.75	–1050.0	23	470.75	1050.0
10	–175.25	–1050.0	24	162.75	1050.0
11	139.25	–1050.0	25	–101.25	1024.5
12	407.25	–1045.0	26	–819.25	988.5
13	725.25	–1045.0	27	–1023.25	988.5
14	910.25	–1045.0			

Pad Description

Pad No.	Pad Name	I/O	Internal Connection	Descriptions
1~3	$\overline{CS2}$~$\overline{CS0}$	O	CMOS Pull-High	Chip selection for the external serial ROM
4	PWR	O	CMOS Pull-High	For external amplifier power control. When the AUD signal is output, the PWR becomes low to make the external amplifier active.
5	DATA	I	CMOS Pull-High	Serial data intput from the external serial ROM
6	ADDR	O	CMOS Pull-High	Serial address output for the external serial ROM
7	CLK	O	CMOS Pull-High	Serial clock output for the external serial ROM
8	$\overline{CS6}$	O	CMOS Pull-High	Chip selection for the external serial ROM
9~10	R1~R0	O	CMOS	Matrix key scan output
11~14	C0~C3	I	Pull-High	Martix key scan input with wake-up function
15	FLAG	O	CMOS	End-pulse output or flash busy output by the code option, active low
16	VDD	—	—	Positive power supply
17	$\overline{CS4}$	O	CMOS	Chip selection for the external serial ROM
18	OSC2	O	—	Oscillator output
19	OSC1	I	—	Oscillator input
20	VSS	—	—	Negative power supply (GND)
21	$\overline{RES}$	I	Pull-High	Input for reset the chip inside Reset is active at the low-going edge or low level
22~23	R2~R3	O	CMOS	Matrix key scan output
24	AUD	O	PMOS Open Drain	Audio output for the external transistor or amplifier
25	$\overline{CS7}$	O	CMOS Pull-High	Chip selection for the external serial ROM
26	$\overline{CS5}$	O	CMOS Pull-High	Chip selection for the external serial ROM
27	$\overline{CS3}$	O	CMOS Pull-High	Chip selection for the external serial ROM

Absolute Maximum Ratings

Supply Voltage .....–0.3V to 5.5V
Input Voltage..... V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature .....–50°C to 125°C
Operating Temperature .....0°C to 70°C

Electrical Characteristics

(Ta=25°C)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	2.4	—	5	V
I_{DD}	Operating Current	3V	No load, F_{SYS}=3.58MHz	—	1	2.4	mA
		5V		—	1.5	4	mA
I_{STB}	Stand-by Current	3V	No load, Halt mode	—	—	3	μA
		5V		—	—	5	μA
V_{IL}	Input Low Voltage	3V	—	0	—	$0.2V_{DD}$	V
		5V	—	0	—	$0.2V_{DD}$	V
V_{IH}	Input High Voltage	3V	—	$0.8V_{DD}$	—	3V	V
		5V	—	$0.8V_{DD}$	—	5V	V
I_{OL}	FLAG Sink Current	3V	V_{OL}=0.3V	2	—	—	mA
		5V	V_{OL}=0.5V	4	—	—	mA
I_{OL1}	$\overline{CS0}$~$\overline{CS7}$, CLK, ADDR, DATA,PWR,R0~R3, Sink Current	3V	V_{OL}=0.3V	1	—	—	mA
		5V	V_{OL}=0.5V	2.5	—	—	mA
I_{OH}	$\overline{CS0}$~$\overline{CS7}$, CLK, ADDR, DATA, PWR, R0~R3 Output Source Current	3V	V_{OH}=2.7V	–0.8	–1.5	—	mA
		5V	V_{OH}=4.5V	–1.5	–3	—	mA
I_O	Max. AUD Output Current	3V	V_{OH}=0.6V	–1.5	–2	—	mA
		5V	V_{OH}=0.6V	–3	–4	—	mA
T_{KEY}	KEY Debounce Time	5V	F_{SYS}=3.58MHz	33	—	—	ms
T_{END}	FLAG End Pulse Width	5V	F_{SYS}=3.58MHz	—	70	—	ms
T_{FLASH}	FLAG Flash Time	5V	F_{SYS}=3.58MHz	—	125	—	ms
P_{PH}	CS0~CS7, CLK, ADDR, DATA, PWR, $\overline{RES}$, C0~C3 Pull-High Resistance	3V	V_{IL}=0V	25	—	100	KΩ
		5V	V_{IL}=0V	15	—	50	KΩ
F_{SYS}	System Frequency	3V	Crystal or Resonator Oscillator	200	—	2000	KHz
		5V		200	—	4000	KHz
T_{RES}	Reset Pulse Width	—	V_{DD}=5V	5	—	—	μs

Functional Description

The HT82012 is a 3-bit/4-bit ADPCM voice synthesizer LSI. It provides 16 matrix keys and external serial ROM interface. Among the 16 keys (KEY0~KEY15), KEY0 is a stop key. KEY1 can be optioned as a direct or a sequential key. As for the rest 14 keys (KEY2~KEY15), they are used as a direct key exclusively. The customer's voice data and all the key definitions are stored in the external serial ROM.

The customer's voice source can be analyzed and coded through the HOLTEK tools. The encoded data are stored in the external HOLTEK 1Mb/512Kb type serial ROM (HT23CXXX). The number of the serial ROM depends on the customer's voice length, 8 at maximum.

Voice Length

Memory Type	Sampling Rate	ADPCM format	Time
512Kb×8	6K	3-bit	228s
		4-bit	171s
1Mb×8	6K	3-bit	456s
		4-bit	342s

Memory configuration

The HT82012 can interface with the external HOLTEK serial ROM as the data memory. The data memory is divided into 7 blocks. Following is the memory configuration for the HT82012:

00000H	Memory initial register
00001H ⋮ 0000FH	Key option table
00010H	Debounce register
00011H	Check sum register
00012H ⋮ 0002FH	Key start address
00030H ⋮	Key group table
FFFFFH	Voice ROM

The memory initial register defines the type of the serial ROM (1M or 512K), power-on status and FLAG output state. The KEY option table records the various trigger ways of the 15 keys (KEY1~KEY15). As for the block of the KEY start address table, it records the individual address of the 15 keys. However, the memory allocation of the sections in each group is described in the KEY group table. Finally, the voice ROM is for the encoded data storage. Following is a more detailed description for these 7 blocks:

- Memory initial register (00000H)

  The initial register saves the external serial ROM type and the output mode. After the power is turned on or the system is reset, the LSI will read-in the register content to decide the voice ROM type (512K or 1M), LSI power on status, FLAG output status and voice synthesis sampling rate.

Bit	Definition		
D0	Serial ROM type	0	512Kb
		1	1Mb
D1	LSI power on state	0	Enter stand-by
		1	Play key1
D2	FLAG output	0	End pulse
		1	Flash
D3	ADPCM code format	0	3 bit
		1	4 bit
D4~D7	Voice sampling rate	See sampling rate table	

* Serial ROM type

The HT82012 can interface with HOLTEK serial ROM that is 512Kb/1Mb (HT23C512/HT23C010).

D0=0, 512Kb type

D0=1, 1Mb type

* LSI power on status

The D1 bit is to define the LSI power on status. When D1=1, the LSI will play the KEY1 voice one time after the power is turned on or system is reset, and then enters the stand-by state. When D1=0, the LSI enters the stand-by state directly after the power is turned on or system is reset.

* FLAG output

When playing voice, the FLAG pin is actived to output one of the following signals through the code option:

- End pulse output (D2=0)

  When the voice output is complete, the FLAG pin outputs a low pulse. The pulse width is 70ms for F_{SYS}=3.58MHz.

- Flash output (D2=1)

  When voice is playing, the FLAG pin outputs a flash signal to drive an LED. However, when the voice output is terminated, the FLAG pin is set to floating. The flash rate is 8Hz, and the output duty is 50% for F_{SYS}=3.58MHz.

* ADPCM code format

The recorded data can be transformed as 3-bit or 4-bit format ADPCM code and then saved in the external serial ROM. For the 3-bit format (D3=0), the same memory size can be used for saving more longer voice content. As for the 4-bit format (D3=1), the synthesized voice will be more approximate to the initial voice.

* Voice sampling rate

If a better sound quality is required, the sampling rate has to be raised. However, more memory size will be required with the raising of the sampling rate. Following is a table for the sampling rates to be chosen:

D4~D7 --> Define the sampling rate (KHz)

Sampling Rate	D7	D6	D5	D4
4	0	0	0	0
4.5	0	0	0	1
5	0	0	1	0
5.4	0	0	1	1
5.8	0	1	0	0
6	0	1	0	1
6.2	0	1	1	0
6.4	0	1	1	1
6.6	1	0	0	0
6.8	1	0	0	1
7	1	0	1	0
7.2	1	0	1	1
7.4	1	1	0	0
7.6	1	1	0	1
7.8	1	1	1	0
8	1	1	1	1

• Key option table (00001H~0000FH)

The table is to define the keys operation function. Each address of the table registers the different functions of a key. For example, the address 00001H is for defining the KEY1 function, and 0000FH the KEY15 function. Every address of the option table includes 8 bits. The bits are defined as follows:

D0	Define the key group play function	0	Repeat
		1	One time
D1	Define the number of the actived keys	0	Non-last key
		1	Last key
D2	Define the key to be retrigerable or non-retriggerable	0	Retrigger
		1	Non-retrigger
D3	Define the key trigger function	0	One shot
		1	Level hold
D4~D7	Reserved		

* Key group play function

The D0 bit is for defining the key group play function. When D0=1, the corresponding key group is played repeatedly. On the other hand, when D0=0, the corresponding key group is played one time and then stops.

- Repeat function (D0=1)

  In the repeat mode, when one of these 15 keys is pressed, the corresponding key group is repeatedly played until other triggers occur, and is then changed to the next group. Notice that the sound can be stopped when the power is turned off or KEY0 is pressed.

- Play one time function (D0=0)

  In the play-one-time function, when one of the 15 keys is pressed, the according section group is played till it is completely finished. Then, the system enters an idle state. To continue, the corresponding key has to be pressed again, and the according group will come into play, etc.

* The number of the actived keys

  The D1 bit is to define the number of the actived keys. When D1=1 the key is defined to be the last key. When D1=0, is not the last key. For example, if the D1 bit of the KEY5(00005H)is"1",it means that KEY1 ~KEY5 are actived keys and KEY6 ~KEY15 are unactived. In addition, the KEY1 sequential cycle is from KEY1 to KEY5 in sequence.

* Retrigger/Non-retrigger definition

  The D2 bit is for defining the key operation to be retrigger or non-retrigger.

  - Retrigger (D2=0)

    When a key group of KEY1~ KEY15 is being played and the key corresponding to the playing section group is released, the currently playing key group is stopped immediately and the according section group of the newly triggered key comes into play if one of KEY1~KEY15 is pressed at this time. However, when a key group of KEY1~KEY15 is being played but the key corresponding to the playing key group is still held down, the newly triggered key is neglected.

  - Non-retrigger (D2=1)

    In the non-retrigger mode,when one of the 15 keys is pressed, the corresponding key group will not start playing till the currently playing group is complete.

* The key trigger function

  The D3 bit is to define the key trigger function. All of the keys (KY1~KEY15) can be optioned as a "one-shot" key or as a "level-hold" key.

  - One shot key (D3=0)

    As a "one shot" key, when one of the 15 keys is pressed, the according section group comes into play till it is completed. Then, the system enters an idle state.

  - Level hold key (D3=1)

    As a "level hold" key, when one of the 15 keys is pressed and held down, the section group corresponding to the held key is kept playing till that held key is released.

• Debounce Register (00010H)

The debounce register is to define the key debounce time.

D0	0	1	0	1
D1	0	0	1	1
Debounce time	250us	22ms	45ms	180ms
D2~D7	reserved			

• Check Sum Register (00011H)

Used to check and ensure the codes of 00000H to 00010H are correct.

• Key start address (00012H~0002FH)

In the KEY start address table, the exact addresses of the 15 keys (KEY1~KEY15) are recorded. The address is the start position in the key group table. Following is a table describing the correspondence of the 15 keys.

00012H	KEY1_SA [0:7]	KEY1
00013H	KEY1_SA [8:15]	
00014H	KEY2_SA [0:7]	KEY2
00015H	KEY2_SA [8:15]	
00016H	KEY3_SA [0:7]	KEY3
00017H	KEY3_SA [8:15]	
⋮	⋮	⋮
0002EH	KEY15_SA [0:7]	KEY15
0002FH	KEY15_SA [8:15]	

• KEY group table (00030H~)

The KEY group table records the memory allocation and functions of the 15 keys. For example, the section start address and section length are defined. What's more, the command register recording the repeat cycle (1 to 16), normal/end section and normal/silence are registered as well. Following is an illustration of the KEY group table:

00030H	SEC_A [0:7]	SEC X	KEY1
00031H	SEC_A [8:15]		
00032H	SEC_A [16:20]		
00033H	SEC_L [0:7]		
00034H	SEC_L [8:15]		
00035H	SEC_L [16:20]		
00036H	Command register		
00037H	Reserved		
⋮	⋮	⋮	
⋮	⋮	SEC Y	
⋮	⋮	⋮	⋮
⋮	⋮	SEC M	
⋮	⋮	⋮	KEY15
⋮	⋮	SEC N	

SEC_A [0:20] : section start address
SEC_L [0:20] : section length

* Voice section and key group

The total synthesized voice contents can be partitioned into the desired number of sections. As for the length of each section, it is decided by the requirements of voice contents.

- Section start address

The encoded voice section is saved in the voice ROM. The section start address is the pointer for the position of current section in the voice ROM. For example, if the voice SECN is saved in the 0000H of the 2nd voice ROM, then the SECN start address is 20000H.

- Section length

The section length is to define the length of the current voice section in the voice ROM. The voice start address can define the end address of the current section on the basis of the voice length in the voice ROM. For example:

The start address: 1000H

The section length: 1F0H

For the 4-bit format, the end address in the voice ROM is 1000+ (1F0/2). As for the 3-bit format, the end address in the voice ROM is 1000 + (1F0/8)×3

- Key group

The HT82012 plays section groups according to the key inputs. Each group can be made up of one or more sections. When a key is triggered, the corresponding section group comes into play. For example, triggering KEY2 plays section group 2, and so forth. The same section is allowed to appear in different groups. KEY1 can be made up of multiple groups when the actived keys are more than 2. Otherwise, each key is comprised by one group only.

* Command register

The command register is to define the voice section repeat number and voice section type.

D0~D3	Voice section repeat number
D4~D5	Voice section type
D6~D7	Reserved

- Voice section repeat number

The same voice section can be repeatedly played for saving the space of the memory. The repeat cycle can be set as 1 to 16 by D0~D3 bits.

Repeat No.	D0	D1	D2	D3
1	0	0	0	0
2	1	0	0	0
: :	: :	: :	: :	: :
15	0	1	1	1
16	1	1	1	1

- Voice section type

The bits of D4 and D5 are used to define the section type as a voice section. silence section or end section.

D5	D4	Type
0	0	Voice section
1	0	Silence section
X	1	End section

• Voice ROM algorithm

A section when triggered by a key input can be played one time, repeated or cascaded with other sections according to the key function table instructions. Following is some example of the section division:

group1:	section4+section2
group2:	section1+section3+section5
: :	: :
group13:	section2
group14:	section7+section5+section1+ section4
group15:	section5

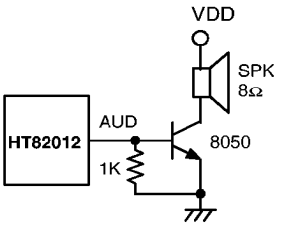
Notice that when one of the included keys groups in the HT82012 is triggered, the voice section(s) of the triggered key group are played in sequence.

AUD

The AUD pin is a PMOS open drain structure. It outputs voice signals to drive the speaker through an external NPN transistor or external power amplifier when the chip is active. However, the AUD pin is floating when the chip is in the stand-by state.

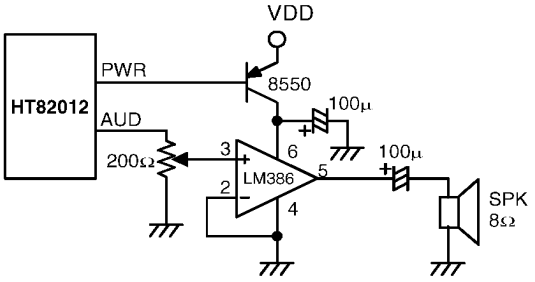
* For transistor

  The 8050 type transistor with $h_{FE} \cong 150$ is recommended to be used as an output driver.



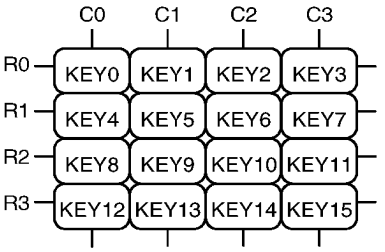
* For power amplifier

  For the power amplifier application, the HT82012 provides a PWR pin to control the power dissipation in stand-by state. For more well audio frequency response and more power for speaker output, the external power amplifier is necessary.



Key trigger mode

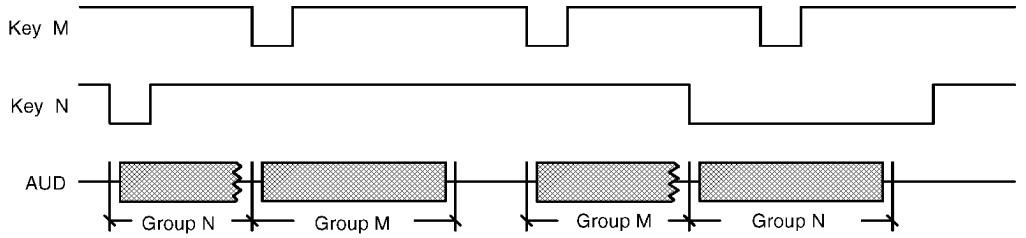
The HT82012 receives direct key trigger input by using a 4×4 keypad. The key matrix is constructed by C0~C3 and R0~R3. In the stand-by mode C0~C3 are all high and no sound is output. When a key is pressed, C0 to C3 starts scanning to detect which key is pressed. The output sound is specified by the according key function table of the pressed key. Notice that when a key is pressed and held down, other key inputs are inhibited.



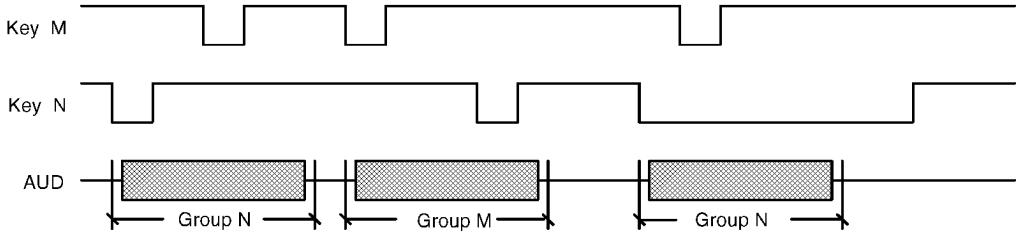
KEY0 is a stop key.

Timing Diagram

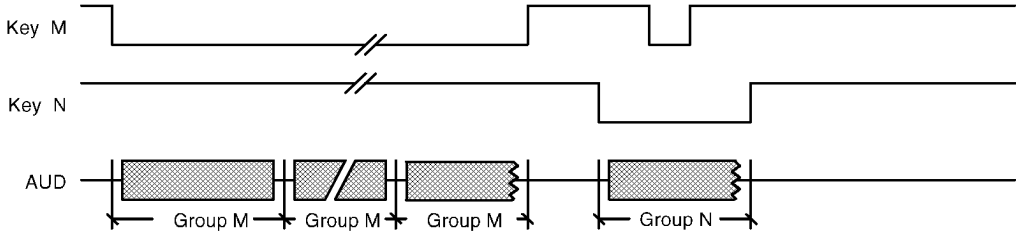
- One shot & retrigger



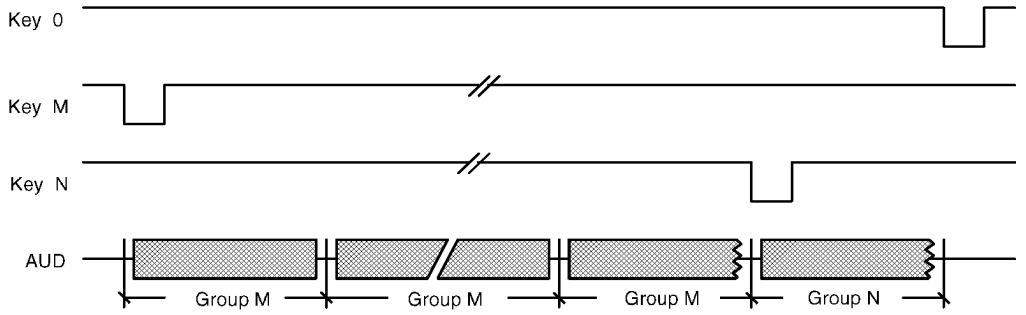
- One shot & non-retrigger



- Level hold

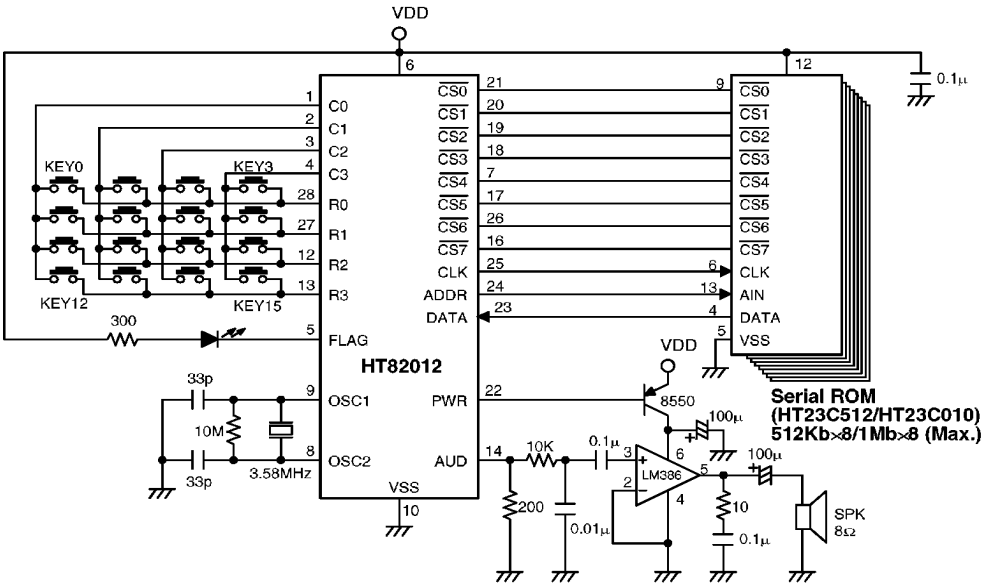


- Repeat & retrigger

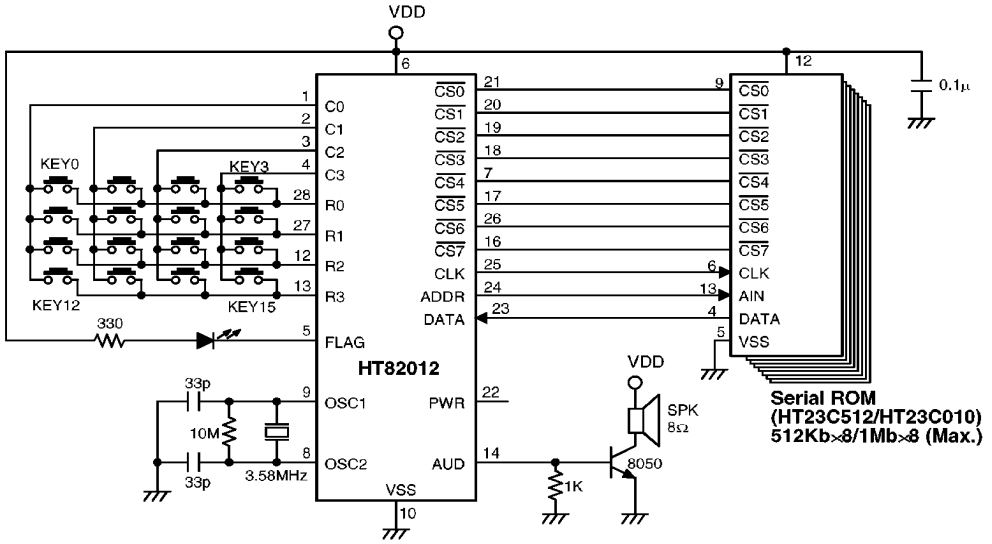


Application Circuit

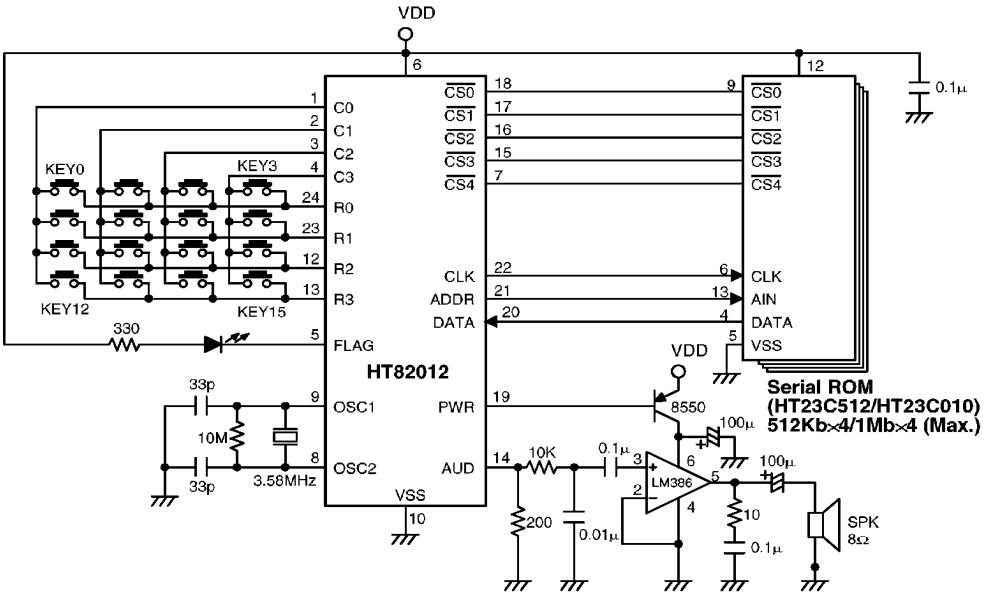
Application with LM386 AMP (28 Pin)



Application with transistor (28 Pin)



Application with LM386 AMP (24 Pin)



Application with transistor (24 pin)